The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte BIRENDRA N. AGARWALA, ERIC M. COKER, ANTHONY CORREALE, JR., HAZARA S. RATHORE, TIMOTHY D. SULLIVAN and RICHARD A. WACHNIK

Appeal No. 2006-1663
Application No. 09/871,883
Technology Center 2800

Decided: September 15, 2006

Before KIMLIN, GARRIS and WALTZ, *Administrative Patent Judges.*

GARRIS, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on an appeal, which involves claims 1-4, 6-13, 15-20, 22-25, and 27-35.

We AFFIRM-IN-PART.

The subject matter of this appeal is drawn to a dual damascene via interconnect structure in a dielectric layer. (Specification, page 1, lines 3-6).

Further details regarding this subject matter are set forth in representative independent claims 1, 10, 20, 25, 30 and 31[1] which read as follows:

1. An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and a lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer,

an upper level wire having a side and a bottom, said upper level wire comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire, at least a portion of the bottom of said upper level wire extending below a top surface of said lower wire level; and

said upper conductive liner in contact with said lower core conductor and also in contact with both the inner surface and the outer surface of said upper edge of said conductive liner in a liner-to-liner contact region.

10. An interconnect structure comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and a lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire, said lower conductive liner having an upper edge having an inner surface, an

[1] In each of the claims the phrase, "said lower wire level" has been construed to mean the "lower level wire". The terms "wire" and "level" appear to be transposed in the claims.

outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom and a via integrally formed in the bottom of said upper level wire, said via have a side and a bottom, said upper level wire and said via each comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire and on the side and bottom of said via, at least a portion of the bottom of said via extending below a top surface of said lower wire level; and

said upper conductive liner on the bottom of said via in contact with said lower core conductor and also in contact with both the inner surface and the outer surface of said upper edge of said lower conductive liner in a liner-to-liner contact region.

20. An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and a lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom and an array of vias integrally formed in the bottom of said upper level wire, each via of said array of vias having a side and a bottom, said upper level wire and each via comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire and on the side and bottom of each via, at least a portion of the bottom each via extending below the top surface of said lower wire level; and

said upper conductive liner on the bottom of each via of a first portion of said array of vias in contact with said lower core conductor and each via of a second portion of said array of vias in contact with said lower core conductor and also in contact with both the inner

surface and the outer surface of said upper edge of said lower conductive liner in liner-to-liner contact regions.

25. An interconnect structure, comprising:

a lower level wire in a dielectric layer, said lower level wire having a side and a bottom and one or more integral extensions each extension having a side and a bottom and extending laterally from the side of said lower level wire, said lower level wire and extensions comprising a lower core conductor and an lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire and said extensions, said lower conductive liner having an upper edge having an inner surface, an outer surface, and a top surface, the top surface of said upper edge substantially coplanar with a top surface of said dielectric layer;

an upper level wire having a side and a bottom and an array of vias integrally formed in the bottom of said upper level wire, each via of said array of vias having a side and a bottom, said upper level wire and each via comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire and on the side and bottom of each via, at least a portion of the bottom each via extending below a top surface of said extensions of said lower wire level; and

said upper conductive liner on the bottom of each said via of a first portion of said array of vias in contact with said lower core conductor of said lower level wire and a second portion of said array of vias in contact with said lower core conductor of said extensions and also in contact with both the inner surface and the outer surface of said upper edge of said lower conductive liner of said extensions in liner-to-liner contact regions.

30. An interconnect structure, comprising:

a lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and a lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire;

one or more dielectric pillars formed in said lower level wire, said lower conductive liner on sides of said dielectric pillars;

an upper level wire having a side and a bottom; said upper level wire comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire; and

said upper conductive liner in contact with said lower core conductor and also in contact with said lower conductive liner on the sides of said dielectric pillars in liner-to-liner contact regions.

31. An interconnect structure, comprising:

a lower level wire having a side and a bottom, said lower level wire comprising a lower core conductor and an lower conductive liner, said lower conductive liner on the side and the bottom of said lower level wire;

one or more dielectric pillars formed in said lower level wire, said lower conductive liner on sides of said dielectric pillars;

an upper level wire having a side and a bottom and one or more vias integrally formed in the bottom of said upper level wire, each via having a side and a bottom, said upper level wire and each via comprising an upper core conductor and an upper conductive liner, said upper conductive liner on the side and the bottom of said upper level wire and on the side and bottom of each via; and

said upper conductive liner on the bottom of at least a portion of said one or more vias in contact with said lower core conductor and at least a portion of said one or more vias in contact with said lower conductive liner on said side of a least a portion of said one or more dielectric pillars in liner-to-liner contact regions.

The references set forth below are relied upon by the Examiner as evidence of obviousness:

Havemann	US 6,156,651	Dec. 5, 2000
Otsuka	US 6,373,136	Apr. 16, 2002
Farrar	US 6,376,370	Apr. 23, 2002

Claims 1-4, 6-13, 15-20, 22-25 and 27-29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Farrar in view of Havemann.

Claims 30-33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Farrar in view of Otsuka.

Claims 34-35 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Farrar in view of Otsuka and further in view of Havemann.

Rather than reiterate the respective positions advocated by the Appellants and by the Examiner concerning these rejections, we refer to the corrected Brief (filed April 25, 2005), Reply Brief (filed November 14, 2003) and Reply Brief responsive to the Supplemental Examiner's Answer (filed September 28, 2005), and to the Answer and Supplemental Examiner's Answer, respectively, for a complete exposition thereof.

OPINION

Appellants have separately argued the following claims: 1, 7-8, 10, 16-18, 20, 23-24, 25, 28-29, 30-31, 32, 33 and 34-35. We shall address these claims accordingly in our opinion below.

The claims are generally directed to an interconnect structure used in semiconductors. To aid in explaining the claimed subject matter, we expound upon claim 1, the broadest claim, by referring to Appellants' Figures 4A and 4B. These figures are reproduced below. We parenthetically note next to the respective claim feature the reference numeral of the particular claim feature referred to in Figures 4A or 4B.

Claim 1 recites a lower level wire (200) in a dielectric layer (245), said lower level wire (200) having a side and a bottom, said lower level wire comprising a lower core conductor (220) and a lower conductive liner (215), said

lower conductive liner (215) on the side and the bottom of said lower level wire (200), said lower conductive liner having an upper edge (285) having an inner surface (290A), an outer surface (290B), and a top surface (290C), the top surface (290C) of said upper edge (285) substantially coplanar with a top surface of said dielectric layer (245); an upper level wire (205) having a side and a bottom, said upper level wire (205) comprising an upper core conductor (230) and an upper conductive liner (225), said upper conductive liner (225) on the side and the bottom of said upper level wire (205), at least a portion of the bottom of said upper level wire (205) extending below a top surface of said lower level wire (200); and said upper conductive liner (225) in contact with said lower core conductor (220) and also in contact with both the inner surface (290A) and the outer surface (290B) of said upper edge of said conductive liner (215) in a liner-to-liner contact region.

Appellants' Figures 4A and 4B are reproduced below:

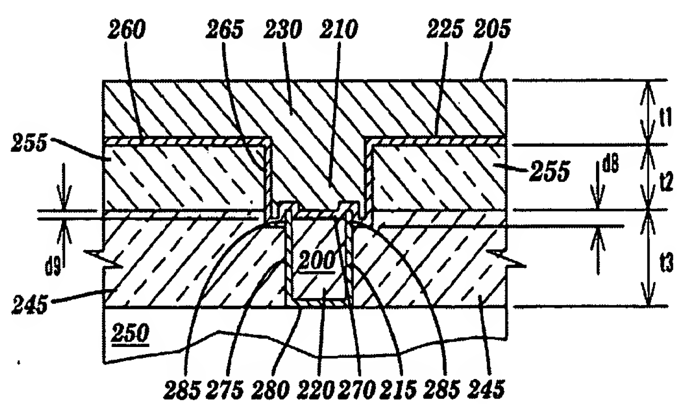

FIG. 4A

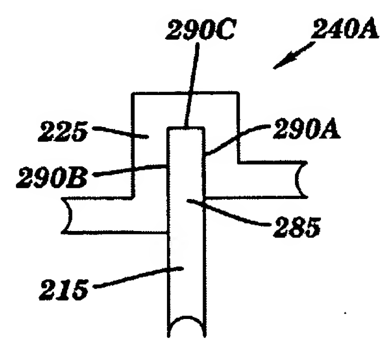

FIG. 4B

Appellants' Figure 4A depicts a cross-sectional view of an embodiment of Appellants' dual-damascene via interconnect.

Appellants' Figure 4B depicts an enlarged view of one upper edge (285) of conductive liner (215) illustrated in Figure 4A.

Independent claims 10, 20, 25, 30 and 31 include various additional claim features while retaining the essential features of claim 1. Appellants' figures that correspond to the embodiment being claimed in the particular independent claim under consideration will be noted in parentheses following the section heading in the opinion.

35 U.S.C. § 103(A) REJECTION: FARRAR IN VIEW OF HAVEMANN

CLAIM 1 (FIGURES 4A AND 4B)

The Examiner rejects independent claim 1 over Farrar in view of Havemann. (Answer 4). The Examiner explains in his rejection that Farrar teaches all the features of claim 1, except "a portion of the bottom of the upper level wire extending below a top surface of the lower wire level, [and] the upper conductive liner in contact with the inner or outer surface of the upper edge of the conductive liner . . . ." (Answer 5). To meet these missing claim features, the Examiner combines Havemann's interconnect structure shown in Figure 3G with Farrar.

Havemann discloses an interconnect structure having an "upper level wire" with an encapsulation layer 48 (i.e., upper conductive liner), conductor metal 52 (i.e., upper core conductor), and a "lower level wire" with via metal 39 (i.e., lower core conductor) and encapsulation material 36 (i.e., lower conductive liner). (Answer 5). The Examiner determines that a portion of "the bottom of the upper level wire [sic, i.e., (encapsulation layer 48)] extends below a top surface of the lower wire level [sic, i.e., (encapsulation material 36)]" as shown in Havemann's Figure 3G. (Answer 5). Also from the overlap of encapsulation layer 48 (i.e.,

upper conductive liner) and encapsulation material 36 (i.e., lower conductive liner) shown in Figure 3G, the Examiner states:

> The upper conductive liner [sic, encapsulation layer 48] is in contact [sic, with] the lower core conductor [sic, via metal 39] and also in contact with the inner surface of [sic, or] outer surface or both surfaces of the upper edge of the conductive liner (see how the upper liner [sic, encapsulation layer] 48 overlaps the upper edge and sides of the lower liner [sic, encapsulation material] 36. (Answer 5).

From the foregoing findings, the Examiner concludes that it would have been obvious to have modified Farrar's liner-to-liner contact region by using Havemann's overlapping interconnect structure to form a contact "without mechanical defects." (Answer 6).

Appellants argue that neither Farrar nor Havemann teaches "at least a portion of the bottom of said upper level wire extending below a top surface of said lower wire level." (Br. 8). Appellants contend that Havemann's encapsulation layer 48 (i.e., upper conductive liner) is not conductive because Havemann indicates that encapsulation layer 48 is made of silicon nitride. (Br. 9). Appellants contend that, since the encapsulation layer 48 is non-conductive, Havemann does not satisfy the claimed upper conductive liner feature. (Br. 9). Moreover, Appellants argue the following: (1) the Examiner does not provide any reason "for combining Farrar with Havemann, (2) the Examiner bases the combination of Havemann with Farrar on the assumption that Havemann teaches forming a contact "without mechanical defects", whereas Havemann teaches forming a contact "without deleterious mechanical effects", (3) one of ordinary skill in the art would not know from Havemann's disclosure which aspects are responsible for forming insulating and conducting layers without deleterious mechanical effects, and (4)

the Examiner does not indicate where Farrar discloses that the insulating and conducting layers suffer from deleterious mechanical effects so as to require Havemann's teachings to remedy such deleterious effects. (Br. 9-11).

Appellants' arguments are not persuasive. We agree with the Examiner's assessment of the conductivity of Havemann's encapsulation layer 48 (i.e., upper conductive liner). (Answer 10). We add that Havemann discloses that silicon nitride is merely an example of the material that may be used as the encapsulation material 48 (i.e., upper conductive liner), not that silicon nitride must be used as the encapsulation material. (Havemann, col. 4, ll. 65-67, "Encapsulation layer 48 (**e.g.**, 0.10 micron of silicon nitride) . . . ." emphasis added). Moreover, Havemann discloses that if silicon nitride is used as the encapsulating material 48 then it would have to be "selectively removed (e.g., from any bottom portion where the conductor is to make electrical contact to via metal)." (Havemann, col. 4, ll. 13-16). Havemann also discloses that electrical contact is established between conductor metal (i.e., upper core conductor) 52 and via metal (i.e., lower core conductor) 39 in the embodiment shown in Figure 3G. (Havemann, col. 5, ll. 9-11). All of Havemann's disclosures indicate that electrical contact is established between conductor metal 52 and via metal 39, even if silicon nitride is used as the encapsulation layer 48.

In order for electrical contact to be established between the conductor metal 52 (i.e., upper core conductor) and the via metal 39 (i.e., lower core conductor) without the added step of "selectively" removing the silicon nitride when it is used as the encapsulation layer (i.e., upper conductive liner) 48, one would have obviously made encapsulation layer 48 (i.e., upper conductive liner) conductive. While Havemann discloses silicon nitride as an example of encapsulation material

48, Havemann's disclosure, as a whole, teaches that it is desired to form electrical contact between the conductor metal 52 (i.e., upper core conductor) and metal via 39 (i.e., lower core conductor) such that it would have been obvious to eliminate the insulative silicon nitride in favor of a conductive encapsulation material for encapsulation layer 48 to thereby obtain such a desired feature.

Additionally, using a conductive material as the encapsulation material 48 (i.e., upper conductive liner) would save an additional step (i.e., the additional selective removal step for the insulative silicon nitride taught by Havemann). (Havemann, col. 4, ll. 12-16, 65-66, col. 5, ll. 9-12). One less step in the method would translate into monetary and time savings for the user, which further evinces the obviousness of using a conductive material for encapsulation layer 48.

From the foregoing explanation, it is our determination that Havemann teaches, or at least would have suggested, the claimed feature: "said upper conductive liner on the side and the bottom of said upper level wire, at least a portion of the bottom of said upper level wire extending below a top surface of said lower wire level."[2]

Contrary to Appellants' argument that the Examiner provides no reason for combining "Farrar with Havemann," the Examiner provides motivation directly from Havemann's disclosure. Specifically, Havemann discloses that connecting the layers in the manner described "realizes desirable insulating and conducting layers without deleterious mechanical effects." (Havemann, abstract).

---

[2] Havemann shows encapsulation layer (i.e., upper conductive liner) 48 extending below the top surface of the edge of the encapsulation material (i.e., lower conductive liner) 36. (Havemann, Figure 3G, reference numerals 36 and 48).

In our view, this disclosure would have motivated one of ordinary skill in the art at the time the invention was made to combine Havemann's overlapping encapsulation material structure with Farrar's barrier layer-to-barrier layer contact region to produce an interconnect structure without deleterious mechanical effects.

As the Examiner notes, Havemann discloses that his invention produces insulating and conducting layers in semiconductors without deleterious mechanical effects. (Havemann, abstract). Havemann's disclosure relating to forming the insulating and conducting layer "without deleterious mechanical effects" includes forming the overlapping encapsulation material structure shown in Figure 3G (i.e., encapsulation layer (i.e., upper conductive liner) 48 and encapsulation material (i.e., lower conductive liner) 36). In looking at the prior art as a whole, Havemann indicates the desirability of using his overlapping encapsulation material structure to provide a more robust dielectric layer, and insulating and dielectric layers without deleterious mechanical effects. (Havemann, abstract). From the foregoing, Havemann provides motivation for the combination with Farrar, that is, to produce layers "without deleterious mechanical effects."

Appellants' argument that one of ordinary skill would not know from Havemann's disclosure which aspects are responsible for forming layers "without deleterious mechanical effects" is not persuasive. As part of Havemann's description to form the layers "without deleterious mechanical effects," Havemann discloses the overlapping encapsulation material structure of Figure 3G. We find that one of ordinary skill in the art reading Havemann's disclosure would have understood that using the overlapping encapsulation material structure of Figure 3G would yield beneficial mechanical effects in the insulating and conducting layers. Moreover, we find that the overlapping encapsulation material structure

shown by Havemann in Figure 3G provides a greater surface area contact between the encapsulation layer (i.e., upper conductive liner) 48 and the encapsulation material (i.e., lower conductive liner) 36. Due to the increased surface area contact, the electrical connection would be enhanced with the added beneficial mechanical effect of providing a stronger joint in the encapsulation material-to-encapsulation material contact area (i.e., the chance of damage to the stronger overlapped encapsulation material-to-encapsulation material interconnection would be reduced by using the overlapping structure).

Appellants make much ado about the Examiner's paraphrasing Havemann's disclosure of forming layers "without deleterious mechanical effects" to mean forming layers "without mechanical defects." (Br. 9-10). However, any error created by such paraphrasing is harmless and certainly does not vitiate the above discussed motivation for combining Havemann with Farrar.

Appellants also argue that the Examiner does not indicate where Farrar discloses insulating and conducting layers having deleterious mechanical effects such that Havemann would be combined with Farrar to cure those deleterious effects. (Br. 10-11). Appellants appear to be arguing that there is no motivation to combine Havemann with Farrar. For reasons previously explained, an artisan would have been motivated to combine the teachings of these references in the manner proposed by the Examiner.

We affirm the § 103(a) rejection of claim 1 and of non-argued claims 2-4, 6, and 9, which depend therefrom.

CLAIMS 7-8

Claim 7 recites that the "liner-to-liner contact region further comprises a second portion co-extensive with said lower conductive liner on a portion of a second side of said lower level wire under said upper level wire." Claim 8 recites that the "liner-to-liner contact region further comprises a third portion co-extensive with said lower conductive liner on an end of said lower level wire under said upper level wire."

The Examiner has rejected claims 7-8 over Farrar in view of Havemann. The Examiner states that Havemann discloses the following:

> The liner-to-liner contact region also comprises a second portion (overlap portion of liner [sic, (i.e., encapsulation layer)] 48) co-extensive with the lower liner [sic, (i.e., encapsulation material 36)] on a portion of a second side (outer portion of liner [sic, (i.e., encapsulation material)] 36) of the lower level wire and a third portion (overlap portion of liner [sic, (i.e., encapsulation layer)] 48 in the hole) co-extensive with the lower conductive liner [sic, (i.e., encapsulation material 36)] on an end (inner portion of the liner [sic, (i.e., encapsulation material)] 36) of the lower level wire, each portion being under the upper level wire. (Answer, pages 5-6).

The Examiner concludes that it would have been obvious to modify the barrier layer-to-barrier layer (i.e., liner-to-liner) contact region of Farrar by adding the second and third coextensive portions as taught by Havemann to form a contact "without mechanical defects." (Answer 6).

Appellants reiterate their argument that Havemann's encapsulation layer (i.e., upper conductive liner) 48 is non-conductive because it is made of silicon nitride. (Br. 12). According to Appellants, because encapsulation layer 48 (i.e., upper conductive liner) is non-conductive it cannot meet the claim feature of an "upper conductive liner."

We addressed this argument above in our discussion of claim 1. This argument is given the same disposition (i.e., unpersuasive) with regard to 7-8.

We affirm the § 103(a) rejection of claims 7 and 8.

CLAIM 10 (FIGURES 4A AND 4B)

The Examiner rejects claim 10 over Farrar in view of Havemann. Claim 10 is substantially the same as claim 1, except that claim 10 further recites that the upper level wire has a "via" integrally formed in the bottom of the upper level wire, the upper conductive liner covers the side and bottom of the via, at least a portion of the via extends below a top surface of the lower wire level, and the upper conductive liner on the bottom of the via is in contact with inner and outer surface of the "liner-to-liner" contact region. (Figure 4A, reference numeral 210 is the "via").

Appellants argue that neither Farrar nor Havemann teach "at least a portion of the bottom of a via extending below a top surface of said lower wire level." (Br. 13). Appellants contend that the Examiner does not identify a "via" in Havemann and the Examiner provides no reason for combining Farrar with Havemann for the claimed portion of the "via" extending below a top surface of the lower wire level. (Br. 13). Appellants also reiterate their arguments made with respect to claim 1.[3]

[3] Appellants again make the following arguments: 1) that combination of Farrar with Havemann is flawed because the Examiner bases his reason for combining Havemann with Farrar on Havemann's teaching to form insulating and conducting layers "without mechanical defects" while Havemann actually teaches forming layers "without deleterious mechanical effects", 2) Havemann does not indicate which aspects of his methodology are responsible for realizing insulating and conducting layers without deleterious mechanical effects, and 3) the Examiner does not indicate where Farrar discloses that the insulating and conducting layers suffer from deleterious mechanical effects so as to require Havemann's teachings

Appellants' argument that the Examiner does not cite where Havemann teaches a "via" is not persuasive. (Br. 13). Havemann discloses that his method forms "mechanically robust vias" (Havemann, abstract). Moreover, Havemann discloses that Figures 3A to 3G, the embodiment used by the Examiner in his rejection, show an "encapsulation type process for vias and conductors." (Havemann, col. 4, ll. 55-56). Thus, Havemann clearly discloses vias in the Figure 3A to Figure 3G embodiment.

The claim feature "at least a portion of the bottom of a via extending below a top surface of said lower wire level" (claim 10) is similar to the claim feature, "at least a portion of the bottom of said upper level wire extending below a top surface of said lower wire level" (claim 1). As aforementioned, Havemann teaches a "via." As we noted with respect to claim 1, Havemann discloses "a portion of the bottom of said upper level wire extending below a top surface of said lower wire level", and there is motivation provided by Havemann to combine such a feature with Farrar.[4] Accordingly, Havemann discloses the "via" feature of claim 10 (i.e., "at least a portion of the bottom of a via extending below a top surface of said lower wire level.").

Contrary to Appellants' argument that the Examiner provides no reason for combining "Farrar with Havemann" for the "at least a portion of the bottom of the via extending below a top surface of said lower wire level" feature, the Examiner provides motivation for combining Havemann's overlapping encapsulation

---

to remedy such deleterious effects. (Br. 13-15). We addressed these arguments in our discussion of claim 1 above. Our reasons for being unconvinced by these arguments also applies to claim 10.

[4] See our discussion of claim 1 for a complete exposition of our position with respect to this claim language.

material-to-encapsulation material structure with Farrar's via configuration (i.e., in Farrar's Figure 3G, reference numeral 328 are vias, and in Figure 3K, reference numeral 334 (i.e., upper conductive liner) coats the inside of via 328 and contacts the barrier layer 314 (i.e., lower conductive liner)). Havemann's overlapping encapsulation layer 48 (i.e., upper conductive liner) with encapsulation material 36 (i.e., lower conductive liner) structure is combined with Farrar's "liner-to-liner contact region" (i.e., barrier/adhesion layers 334 and 314 in Figure 3K) to produce an interconnect structure "without mechanical defects" (i.e., without deleterious mechanical effects). (Answer 6). Moreover, the motivation the Examiner provides is found in the disclosure of Havemann. (Answer 6, Havemann, abstract).

We affirm the § 103(a) rejection of claim 10 and non-argued claims 11-13, 15 and 19, which depend therefrom.

CLAIMS 16-18

Claim 16 requires the liner-to-liner contact region to have a second portion co-extensive with said lower conductive liner on a portion of a second side of the lower level wire under the via. Claim 17 recites the liner-to-liner contact region has a third portion coextensive with the lower conductive liner on an end of the lower level wire under the via. Claim 18 recites the liner-to-liner contact region comprises a first portion coextensive with the lower conductive liner on a portion of a first side of the lower level wire under the via and a second portion coextensive with said lower conductive liner on a portion of an end of said lower level wire under said via.

The Examiner rejects claims 16-18 under 35 U.S.C. § 103(a) over Farrar in view of Havemann. It is apparent that the Examiner applies the same rationale

from the rejection of claims 7-8 to claims 16-18. (Answer 6, See, CLAIMS 7-8 section above).

Appellants again argue that Havemann's encapsulation layer 48 (i.e., upper conductive liner) is not conductive because it is disclosed as being made of silicon nitride. (Br. 16-17). According to Appellants, Havemann does not teach or suggest the upper conductive liner claim feature. Appellants also argue that the Examiner does not state anything regarding the coextensiveness of the liner under a via because he fails to indicate that Havemann even teaches a via. (Br. 16). Appellants' arguments are not persuasive.

Earlier in this opinion, we addressed Appellants' argument regarding the conductivity of encapsulation layer 48 (i.e., upper conductive liner) with regard to claim 1. Additionally, as we discussed above regarding claim 10, we find that Havemann discloses a via in the embodiment cited by the Examiner (i.e., Figures 3A-3G). Accordingly, we make the same disposition (i.e., unpersuasive) of Appellants' arguments with regard to claims 16-18. (See our discussion of claims 1 and 10 for further explanation).

We affirm the § 103(a) rejection of claims 16-18.

CLAIMS 20 AND 25 (FIGURES 4A AND 12A)

Claim 20 is similar to claim 1, except that claim 20 further recites that the upper level wire has "an array of vias integrally formed in the bottom of said upper level wire" (Figure 12A, reference numerals 210A to 210I), "at least a portion of the bottom of each via extending below the top surface of the lower wire level" (Figure 4A, reference numerals 215 and 225), "a first portion of the array in contact with the lower core conductor" (Figure 12A, reference numerals 330B,

330C) and "a second portion of the array of vias in contact with said lower core conductor and also in contact with both the inner surface and outer surface of said upper edge of said lower conductive liner"(Figure 12A, reference numeral 330A).

Claim 25 is similar to claim 20, except that claim 25 further recites the lower level wire having "one or more integral extensions each extension having a side and a bottom and extending laterally from the side of said lower level wire" (Figure 12A, reference numeral 315A to 315C).

The Examiner rejects claims 20 and 25 under 35 U.S.C. § 103(a) over Farrar in view Havemann. (Answer 4-6).

Appellants make the same arguments with respect to both claims 20 and 25. Appellants' arguments are as follows: (1) neither Farrar nor Havemann teaches the claim feature, "at least a portion of the bottom of each via extending below a top surface of said lower wire level." (Br. 17, 22), (2) Examiner does not indicate any via in Havemann (Br. 17, 22), (3) the Examiner provides no reason for combining Farrar with Havemann (Br., 18, 22), (4) the Examiner incorrectly bases the combination of Havemann with Farrar on the Examiner's statement that Havemann teaches forming contacts "without mechanical defects" (Br. 18, 22-23), (5) Havemann does not disclose which aspects of his method are responsible for realizing insulating and conducting layers without deleterious mechanical effects (Br. 19, 23), and (6) Farrar does not disclose forming layers that have deleterious mechanical effects such that applying Havemann to Farrar would improve Farrar's methodology (Br. 19, 23-24). Appellants' arguments are not persuasive.

Regarding Appellants' argument that neither Farrar nor Havemann teaches the claim feature, "at least a portion of the bottom of each via extending below a top surface of said lower wire level", Havemann clearly indicates that the Figures

3A-3G embodiment, cited by the Examiner in his rejection, teach an encapsulation process for vias. (Havemann, col. 4, lines 55-56). Additionally, Farrar teaches an array of vias (Farrar, Figure 3G, reference numeral 328; i.e., there is a "via" on the right-hand side of the figure and a "via" on the left-hand side of the figure). Moreover, once Havemann's overlapping encapsulation layer structure (i.e., encapsulation layer 48 (i.e., upper conductive liner) and encapsulation material 36 (i.e., lower conductive liner)) is incorporated into Farrar's interconnect via structure, then the encapsulation layer 48 (i.e., upper conductive liner) will extend "below a top surface of said lower wire level" (i.e., Havemann, Figure 3G, encapsulation layer 48 (i.e., upper conductive liner) extends below a top surface of the encapsulation material 36 (i.e., lower conductive liner)). The combination of Havemann's overlapping encapsulation material structure with Farrar's barrier layer-to-barrier layer (i.e., liner-to-liner) structure would result in each via in the array having a bottom that extends below a top surface of the lower wire level.

Arguments (2) through (6) delineated above are not persuasive. Earlier in this opinion, we addressed Appellants' arguments (2) through (6) in our discussion of claims 1 and 10. These arguments regarding claims 20 and 25 are given the same disposition (i.e., unpersuasive) as those arguments applied to claims 1 and 10.

We affirm the § 103(a) rejection of claims 20 and 25, and non-argued claims 22 and 27, which depend therefrom.

CLAIMS 23-24 AND 28-29

Claim 23 recites the "liner-to-liner contact region further comprises second portions co-extensive with said lower conductive liner on portions of second sides of said lower level wire under vias of said second portion of said array of vias." Claim 28 requires that the liner-to-liner contact region have "second portions co-extensive with said lower conductive liner on portions of second sides of said extensions of said lower level wire under vias of said second portion of said array of vias." Claim 24 requires the "liner-to-liner contact region further comprises a third portion co-extensive with said lower conductive liner on an end of said lower level wire under vias of said second portion of said array of vias." Claim 29 recites that the liner-to-liner contact region has "a third portion co-extensive with said lower conductive liner on an end of said lower level wire under vias of said second portion of said array of vias."

The Examiner rejects claims 23-24 and 28-29 under 35 U.S.C. § 103(a) over Farrar in view of Havemann (Answer 4-6).

Appellants reiterate the following arguments they previously made with respect to claims 16-18: (1) Havemann does not disclose vias which are required by claims 23-24 and 28-29 and (2) Havemann's encapsulation layer 48 (i.e., upper conductive liner) is disclosed as being made of silicon nitride which is non-conductive, so Havemann does not disclose an upper conductive liner. These arguments are not persuasive.

We addressed arguments (1) and (2) in our discussion of claims 16-18. The same disposition (i.e., unpersuasive) of those arguments applies to claims 23-24 and 28-29.

Accordingly, we affirm the Examiner's § 103(a) rejection of claims 23-24 and 28-29.

35 U.S.C. § 103(a) REJECTION: FARRAR IN VIEW OF OTSUKA

CLAIMS 30-31 (FIGURE 17 AND FIGURE 18)

Claim 30 is similar to claim 1, except that claim 30 further recites that "one or more dielectric pillars [are] formed in said lower level wire, said lower conductive liner on sides of said dielectric pillars" (Figure 17, reference numeral 365) and "said upper conductive liner [is] in contact with said lower core conductor and also in contact with said lower conductive liner on the sides of said dielectric pillars in liner-to-liner contact regions" (Figure 18, reference numerals 215, 225, 365).

Claim 31 is similar to claim 30, except that it further recites "said upper level wire having . . . one or more vias integrally formed in the bottom of said upper level wire" wherein each via has an upper core conductor and upper conductive liner, the upper conductive liner is on the side and bottom of the upper level wire and on the side and bottom of each via, such that upper conductive liner on the bottom of at least a portion of said one or more vias is in contact with the lower core conductor and at least a portion of said one or more vias is in contact with said lower conducive liner on the sides of at least a portion of one or more dielectric pillars. (Figure 18, reference numeral 210 is the "via"; Figure 17, reference numerals 210 and 365).

The Examiner rejects claims 30-31 under § 103(a) over Farrar in view of Otsuka. The Examiner states "Farrar shows all of the elements of the claims except the dielectric pillars formed in the lower level wire." (Answer 7). The Examiner relies on Otsuka to teach placing insulating pillars (i.e., dielectric pillars)

in a "level of wiring." (Answer 7). The Examiner then concludes that it would have been obvious to "modify the lower interconnect wiring level of Farrar by adding dielectric pillars as taught by Otsuka et al. to form a highly reliable damascene wiring structure" as Otsuka teaches. (Answer 7).

Appellants argue that neither Farrar nor Otsuka discloses the claim feature "lower conductive liner on [the] sides of said dielectric pillars." Appellants also argue the Examiner's reason for combining Otsuka with Farrar (i.e., "to form a highly reliable damascene wiring structure") is not persuasive because Otsuka's improved reliability against void formation is not necessary in Farrar. Farrar uses barrier layers 384 and 314 shown in Figure 3K to prevent void formation. (Br. 26-27). Appellants argue that adding dielectric pillars to Farrar would add an unnecessary expense that Farrar specifically teaches to avoid. (Br. 27).

The Examiner responds that "Otsuka was cited to show that dielectric pillars were formed in a wiring level to improve the structural integrity" of that level. (Answer 12). Moreover, the Examiner determines that "since semiconductors often have many wiring levels, and each wiring level essentially consists of the same structures" one of ordinary skill would find that Otsuka's insulating pillars would also be useful in a lower wiring level. (Answer 12). Furthermore, the Examiner states that Otsuka forms the insulating pillars (i.e., dielectric pillars) in a conductor layer, which would be next to the liner and core conductor. (Answer 12). The Examiner then determines that, when Otsuka and Farrar are combined, the barrier/adhesive layer 314 (i.e., lower conductive liner) would be on the side of one or more insulating pillars (i.e., dielectric pillars) of Otsuka. (Supplemental Examiner's Answer 3).

We agree with Appellants' ultimate position that the § 103(a) rejection over Farrar in view of Otsuka is improper. Otsuka teaches that the insulating pillars P (i.e., dielectric pillars) are placed around a via hole to prevent large crystal growth in the conductor layer. (Otsuka, col. 11, ll. 33-36). Otsuka discovered that when pillars are not used, the smaller crystals with higher surface energy in the via encourage the metal atoms to diffuse out of the via toward the larger crystals with lower surface energy in the conductor layer thereby forming a void in the via. (Otsuka, col. 6, l. 57 to col. 7, l. 6). In contrast, Farrar uses diffusion barrier layers (i.e., Fig. 3K, reference numerals 314 (i.e., lower conductive liner) and 334 (i.e., upper conductive liner)) to prevent or slow the electromigration of copper atoms which ultimately forms an undesirable void. (Farrar, col. 1, ll. 45-52, col. 3, ll. 52-56, col. 15, ll. 9-17, col. 16, l. 12 and col. 19, ll. 42-43). Thus, Otsuka uses a completely different methodology and structure to control electromigration (i.e., insulating pillars (i.e., dielectric pillars) for controlling crystal growth in the conductor layer to control electromigration) than Farrar (i.e., barrier layers to prevent electromigration).

Accordingly, we agree with Appellants' argument that including Otsuka's insulating pillars to control crystal growth, and thereby control electromigration, with Farrar's interconnect structure would be unnecessary because Farrar already provides barrier/adhesive layers 314 and 334 to prevent electromigration. Farrar already provides a solution to the electromigration problem (i.e., the barrier/adhesive layers 314 and 334) which militates against combining Otsuka's insulating pillars to solve a non-existent electromigration problem in Farrar as Appellants advocate. (Br. 27).

Moreover, even if Otsuka's insulating pillars (i.e., dielectric pillars) were to be combined with Farrar's interconnect structure; Appellants' claimed structure would not result. In Otsuka's Figure 13C embodiment cited by the Examiner, the insulating pillars P (i.e., dielectric pillars) are placed in the upper wiring 10. (Otsuka, col. 12, ll. 30-35). Thus, when combined with Farrar, Otsuka's Figure 13C embodiment indicates that the insulating pillars (i.e., dielectric pillars) would be combined with Farrar's second core conductor 344 (i.e., upper core conductor). This teaching is contrary to the express claim language, which requires that the dielectric pillars be "formed in said lower level wire." The Examiner's reasoning that since semiconductors have many layers one would find it useful to place Otsuka's insulating pillars in a lower wiring level (Supplemental Examiner's Answer 2) appears to be based solely on impermissible hindsight.

For the foregoing reasons, the 35 U.S.C. § 103(a) rejection of claims 30 and 31 over Farrar in view of Otsuka cannot be sustained.

CLAIMS 32-33

Claims 32-33 depend from claim 31 and are likewise rejected under 35 U.S.C. § 103(a) over Farrar in view of Otsuka. Because claims 32 and 33 depend from claim 31, the rejections of these claims cannot be sustained for the same reasons the rejection of claim 31 could not be sustained.

Accordingly, we reverse the 35 U.S.C. § 103(a) rejection of claims 32 and 33 over Farrar in view of Otsuka.

CLAIMS 34-35

Claims 34 and 35 depend from claims 33 and 34, respectively. Claim 33, as noted above, depends from claim 31. Claims 34-35 are rejected under 35 U.S.C. § 103(a) over Farrar in view of Otsuka and further in view of Havemann. Because claims 34-35 ultimately depend from claim 31, the rejection of these claims cannot be sustained for the same reasons the rejection of claim 31 could not be sustained.

Accordingly, we reverse the 35 U.S.C. § 103(a) rejection of claims 34 and 35 over Farrar in view of Otsuka and further in view of Havemann.

CONCLUSION

We have affirmed the 35 U.S.C. § 103(a) rejection of claims 1-4, 6-13, 15-20, 22-25 and 27-29 as being unpatentable over Farrar in view of Havemann.

We have reversed the 35 U.S.C. § 103(a) rejection of claims 30-33 as being unpatentable over Farrar in view of Otsuka.

We have reversed the 35 U.S.C. § 103(a) rejection of claims 34 and 35 as being unpatentable over Farrar in view of Otsuka and further in view of Havemann.

The decision of the Examiner is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv)(effective Sept. 13, 2004).

AFFIRMED-IN-PART

BRG:tf

Arlen L. Olsen
Schmeiser, Olsen & Watts
3 Lear Jet Lane
Suite 201
Latham, New York 12110